

based on a value stored in the register.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect the amendment of claim 10, cancellation of claims 1-9 and 11-20, and the addition of new claims 21-40. The specific amendments to individual claims are detailed in the following set of claims.

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Please cancel claims 1-9 and 11-20.

Please amend the following claim:

10. (Once Amended) [The method of claim 9] A method comprising:
storing programmed code on a computer readable medium external to a processor;
executing, by the processor, the programmed code; and
controlling one or more functions of the processor in response to executing the programmed
code, wherein the one or more functions are controlled by directly triggering hardware on the processor in response to executing the programmed code.

Please add the following new claims:

21. (New) A system, comprising:
a bus;
a processor including a plurality of machine specific registers, wherein each one of the plurality of machine specific registers is associated with one or more functional units of the processor; and
a computer readable medium external to the processor and coupled to the processor by the bus, the computer readable medium to store instructions to implement microcode functions which result in changing a value of at least one bit in at least one of the plurality of machine specific registers.
22. (New) The system of claim 1, wherein the computer readable medium is firmware.

23. (New) The system of claim 1, wherein the plurality of machine specific registers includes a bank of registers associated with one of the functional units.
24. (New) The system of claim 1, wherein one of the functional units is an internal bus controller.
25. (New) The system of claim 1, wherein one of the functional units is an internal data cache of the processor.
26. (New) The system of claim 25, wherein the instructions implement microcode functions by updating the at least one of the plurality of machine specific registers.
27. (New) The system of claim 26, wherein the instructions implement microcode functions by setting the at least one bit to invalidate a line of the cache.
28. (New) The system of claim 25, wherein the instructions implement microcode functions by triggering processor hardware logic and by manipulating the plurality of machine specific registers.
29. (New) A method, comprising:
storing microcode on a computer readable medium external to a processor;
executing the microcode using the processor, wherein the processor includes a plurality of machine specific registers associated with at least two functional units of the processor; and
controlling one of the at least two functional units of the processor in response to executing the microcode by modifying a value of at least one bit included in one of the plurality of machine specific registers.
30. (New) The method of claim 29, wherein modifying a value of at least one bit included in one of the plurality of machine specific registers associated with one of the at least two functional units of the processor operates to affect the behavior of an other one of the at least two functional units of the processor.

31. (New) The method of claim 29, wherein a logical source register and a logical destination register for executing an instruction of the microcode are selected from the plurality of machine specific registers.

32. (New) The method of claim 29, wherein the at least two functional units are linked by a communication bus to a data control unit to fetch an instruction of the microcode from the computer readable medium external to a processor.

33. (New) The method of claim 29, wherein controlling one of the at least two functional units of the processor in response to executing the microcode further includes:
controlling a non-performance critical function.

34. (New) The method of claim 33, wherein the non-performance critical function is selected from the group consisting of:
cache flushing, cache invalidation, setting processor features, reading processor features, machine check handling, floating point calculations, processor diagnosis, architecture handling for backward compatibility, authentication, platform management interrupt, diagnostic functions and debug functions.

35. (New) An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:
storing microcode in firmware external to a processor;
executing the microcode by the processor;
updating one or more machine specific registers associated with a logic unit on the processor in response to the executing of the programmed code; and
controlling one or more functions of the logic unit on the processor based on a value stored in the one or more machine specific registers.

36. (New) The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

moving a value from a general purpose register of the processor to the one or more machine specific registers.

37. (New) The article of claim 35, wherein the machine-accessible medium further includes data, which when accessed by the machine, results in the machine performing:

reprogramming the microcode in the firmware.

38. (New) An apparatus, comprising:

a first logic unit; and

at least two machine specific registers associated with the logic unit, the at least two machine specific registers to trigger processor hardware logic functions when a selected one of the at least two machine specific registers is updated in response to executing a microcode instruction fetched from a memory external to the processor.

39. (New) The apparatus of claim 38, further comprising:

a second logic unit associated with a selected one of the at least two machine specific registers.

40. (New) The apparatus of claim 39, wherein changing a value of at least one bit in a selected other one of the at least two machine specific registers affects the behavior of the second logic unit.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 27, 2001, and the references cited therewith. Claims 1-9 and 11-20 are canceled, claim 10 is amended, and claims 21-40 are added. As a result, claims 10 and 21-40 are now pending in this application.

While it was noted that claims 1-20 were rejected on form PTO-326 included in the Office Action, the status of claim 10 was not addressed in the text of the Action, and thus the